LISTING OF CLAIMS

The following is a complete listing of pending claims with a status identifier in parenthesis.

LISTING OF CLAIMS

1. (Previously Presented) A data bus width conversion apparatus for receiving N-bit data (N is a positive integer) from a first device having a first bus width and outputting the N-bit data to a second device having a second bus width, wherein the first device divides the N-bit data into a plurality of bit data groups and the plurality of bit data groups are transferred to the apparatus, the apparatus comprising:

a setting section for setting the total number of transfer operations required for the first device to transfer the plurality of bit data groups, and for setting a division pattern of the N-bit data for dividing the N-bit data into the plurality of bit data groups;

a receiving section for receiving data indicated by each of the plurality of bit data groups in accordance with the total number of transfer operations and the division pattern; and

an output section for producing the N-bit data from the received data indicated by each of the plurality of bit data groups and outputting the produced N-bit data to the second device.

2. (Previously Presented) A data bus width conversion apparatus according to claim 1, wherein the first device divides the N-bit data into the plurality of bit data groups in accordance with the total number of transfer operations and the division pattern set by the setting section.

3. (Previously Presented) A data bus width conversion apparatus according to claim 1, wherein the setting section determines the total number of transfer operations and the division pattern in accordance with an instruction from the first device.

4. (Previously Presented) A data bus width conversion apparatus according to claim 1, wherein the setting section determines the total number of transfer operations and the division pattern in accordance with the size of the first bus width.

5. (Previously Presented) A data bus width conversion apparatus according to claim 1, wherein:

each of the plurality of bit data groups is transferred by the first device in a transfer operation having a prescribed ordinal number within the total number of transfer operations; and

the receiving section comprises:

a counter section for counting the current number of transfer operations within the total number of transfer operations;

a comparing section for comparing the current number of transfer operations with the ordinal number of a transfer operation for each of the plurality of bit data groups; and

a sampling section for sampling the plurality of bit data groups in accordance with a result of the comparison.

6. (Previously Presented) A data bus width conversion apparatus according to claim 5, wherein the counter section resets the number of counts to an initial value after the current ordinal number of a transfer operation reaches the

total number of transfer operations.

7. (Previously Presented) A data bus width conversion apparatus according to claim 1, wherein the setting section comprises:

a first register for setting the total number of transfer operations; and

a second register for setting the division pattern.

8. (Previously Presented) A data bus width conversion apparatus according to claim 1, wherein the apparatus outputs the N-bit data to the second device in data write access from the first device to the second device.

9. (Previously Presented) A data bus width conversion apparatus according to claim 1, wherein the apparatus outputs the N-bit data to the second device in bi-directional data transfer access between the first device and the second device.

10. (Previously Presented) A data bus width conversion apparatus for dividing N-bit data (N is a positive integer) output from a second device having a second bus width into a plurality of bit data groups and transferring the plurality of bit data groups to a first device having a first bus width, the apparatus comprising:

a setting section for setting the total number of transfer operations required for transferring the plurality of bit data groups to the first device, and for setting a division pattern of the N-bit data for dividing the N-bit data into the plurality of bit data groups; and

a dividing section for dividing the N-bit data into the plurality of bit data groups in accordance with the total number of transfer operations and the division

pattern.

11. (Previously Presented) A data bus width conversion apparatus according to claim 10, wherein the apparatus outputs the plurality of bit data groups to the first device in data read access from the second device to the first device.

12. (Previously Presented) A data bus width conversion apparatus according to claim 10, wherein the apparatus outputs the plurality of bit data groups to the first device in bi-directional data transfer access between the first device and the second device.

13. (Previously Presented) A data processing apparatus, comprising:

a data bus width conversion apparatus for receiving N-bit data (N is a positive integer) from a first device having a first bus width and outputting the N-bit data, wherein the first device divides the N-bit data into a plurality of bit data groups and the plurality of bit data groups are transferred to the data bus width conversion apparatus; and

a second device having a second bus width for receiving the N-bit data output from the data bus width conversion apparatus,

wherein the data bus width conversion apparatus comprises:

a setting section for setting the total number of transfer operations required for the first device to transfer the plurality of bit data groups, and for setting a division pattern of the N-bit data for dividing the N-bit data into the plurality of bit data groups;

a receiving section for receiving data indicated by each of the plurality of bit data groups in accordance

with the total number of transfer operations and the division pattern; and

an output section for producing the N-bit data from the received data indicated by each of the plurality of bit data groups and outputting the produced N-bit data to the second device.

14. (Previously Presented) A data processing apparatus according to claim 13, wherein the data processing apparatus is a display apparatus.

15. (Previously Presented) A data processing apparatus, comprising:

a second device having a second bus width for outputting N-bit data (N is a positive integer); and

a data bus width conversion apparatus for dividing the N-bit data output from the second device into a plurality of bit data groups and transferring the plurality of bit data groups to a first device having a first bus width,

wherein the data bus width conversion apparatus comprises:

a setting section for setting the total number of transfer operations required for transferring the plurality of bit data groups to the first device, and for setting a division pattern of the N-bit data for dividing the N-bit data into the plurality of bit data groups; and

a dividing section for dividing the N-bit data into the plurality of bit data groups in accordance with the total number of transfer operations and the division pattern.

16. (Previously Presented) A data processing apparatus according to claim 15, wherein the data processing apparatus is a display apparatus.